Government Girls' Polytechnic, Bilaspur

Name of the Lab: **Digital Electronics Lab**

Practical: **Digital Electronics Lab**

Class :**3rd Semester (ET&T), 3rd Semester (CS)**
FOR ET&T
Teachers Assessment: 10 End Semester Examination: 50
FOR CS
Teachers Assessment: 20 End Semester Examination: 50

List of Experiments

1. Verify Truth Table of Logic Gates (AND, OR, NOT, NAND & NOR Gates).
2. Design Basic Gates Using NAND gates.
3. Design Basic Gates Using NOR gates.
4. Verify Demorgan's Theorem.
5. Design Half Adder. (a) Using AND/OR/NOT Gates. (b) Using NAND/NOR Gates.
6. Design Full Adder.
7. Design Half Subtractor.
8. Design Full Subtractor.
9. Verify the operation of magnitude comparator (7485 IC).
10. Verify the Truth Table of RS Flip-flop, JK F/F, D F/F & T type F/F.
11. Design 3/4 bit Counter & verify truth table.
12. Design a register such that it can be used as a serial/parallel Shift register.